FIG. 1

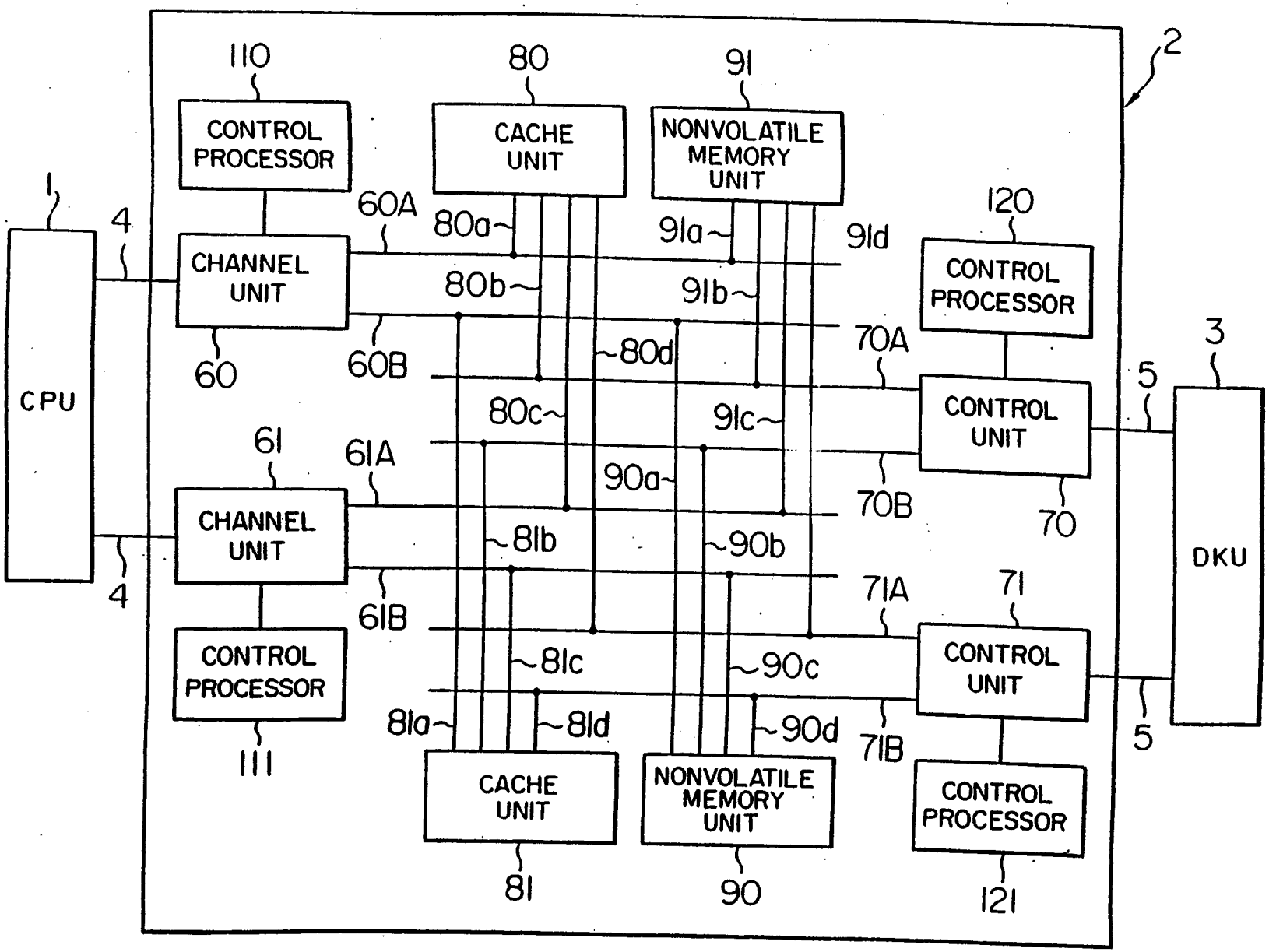

110
80
91
2
CONTROL PROCESSOR
CACHE UNIT
NONVOLATILE MEMORY UNIT
1
4
60A
80a
91a
91d
120
CHANNEL UNIT
80b
91b
CONTROL PROCESSOR
70A
3
CPU
60
60B
80d
5
80c
91c
61
61A
CONTROL UNIT
90a
70B
DKU
CHANNEL UNIT
81b
90b
70
4
71A
71
61B
CONTROL PROCESSOR
81c
90c
CONTROL UNIT
81a
81d
90d
71B
5
CACHE UNIT
NONVOLATILE MEMORY UNIT
CONTROL PROCESSOR
111
81
90
121

FIG. 2

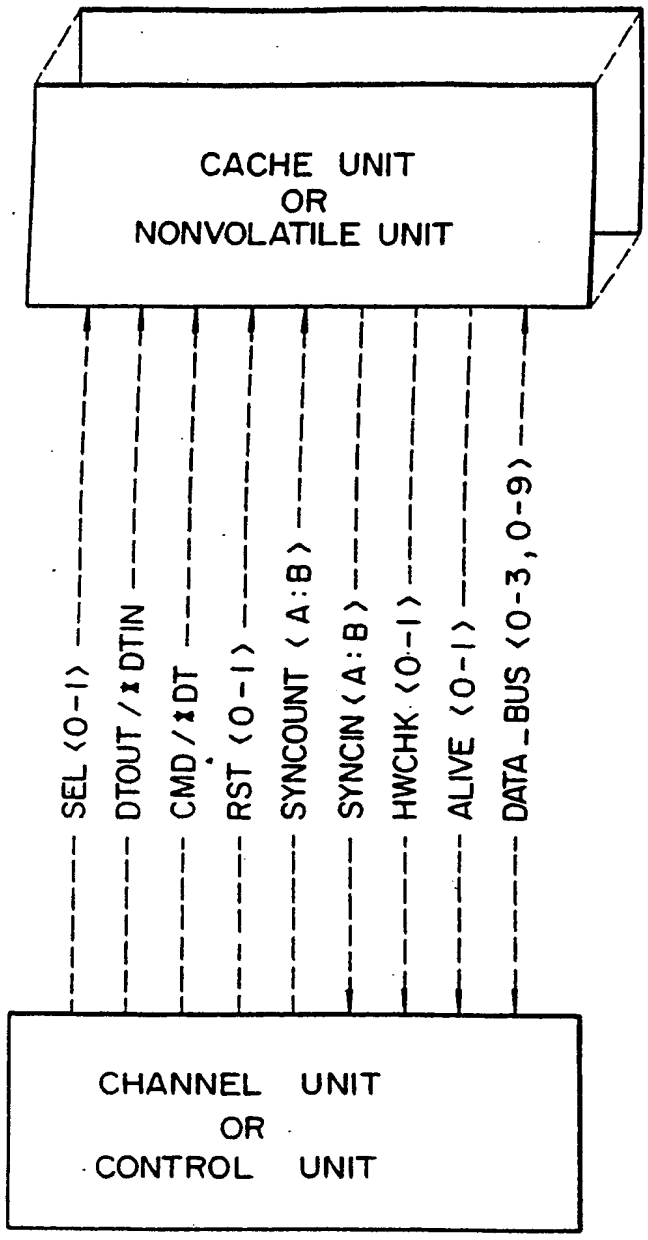

CACHE UNIT
OR
NONVOLATILE UNIT
SEL ⟨0-1⟩
DTOUT / ⁂ DTIN
CMD / ⁂ DT
RST ⟨0-1⟩
SYNCOUNT ⟨A:B⟩
SYNCIN ⟨A:B⟩
HWCHK ⟨0-1⟩
ALIVE ⟨0-1⟩
DATA_BUS ⟨0-3, 0-9⟩
CHANNEL UNIT
OR
CONTROL UNIT

FIG. 3

DATA BUS PROTOCOL

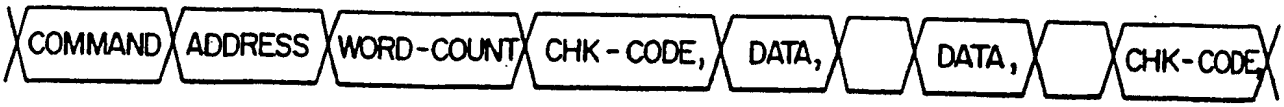


FIG. 4

DATA BUS MODE

DUOUT / $\overline{\text{DTIN}}$	CMD / $\overline{\text{DT}}$	BUS MODE
1	1	TRANSFER COMMAND
1	0	TRANSFER WRITE DATA
0	1	TRANSFER STATUS
0	0	TRANSFER READ DATA

FIG. 5

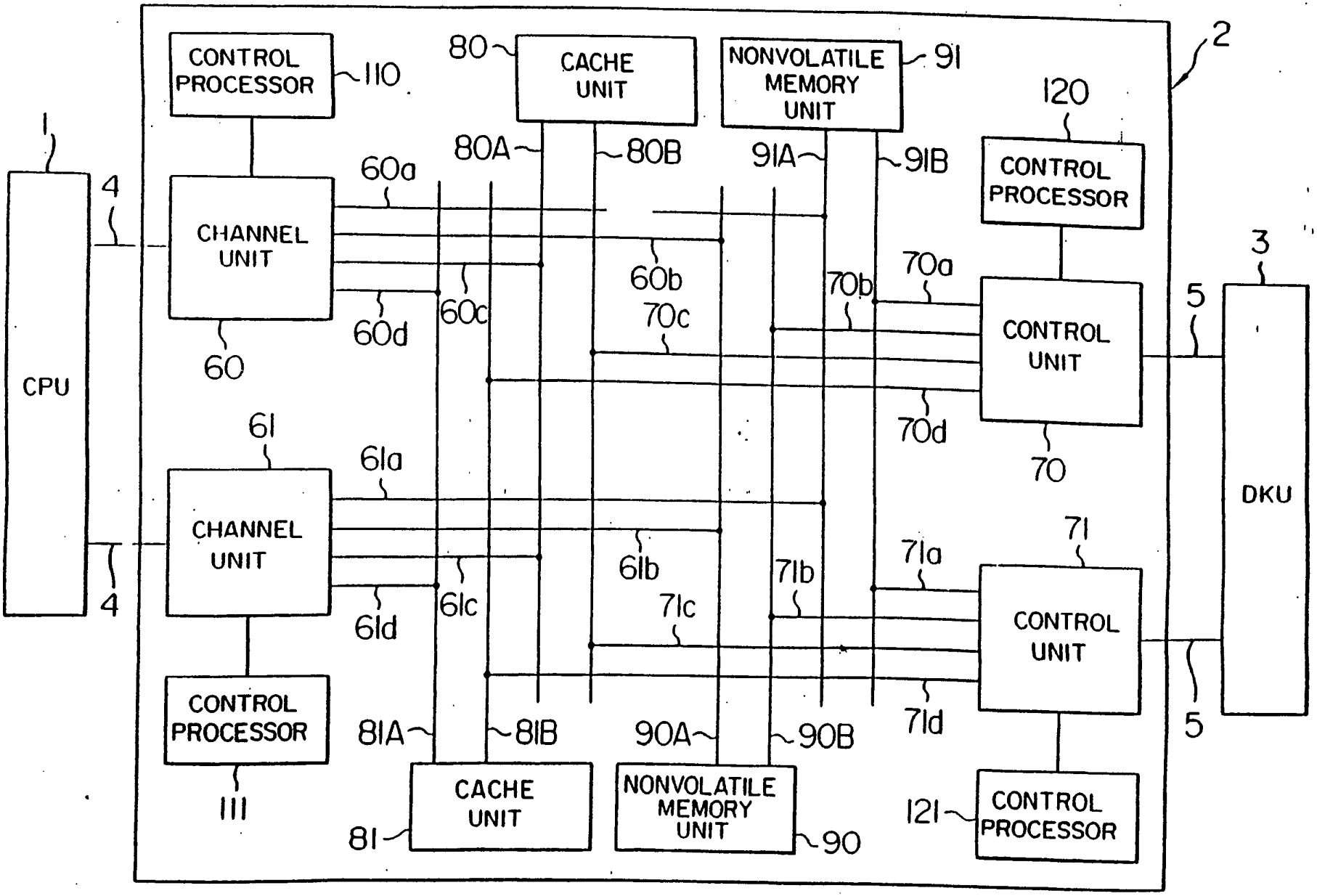

CONTROL PROCESSOR
110
80
CACHE UNIT
NONVOLATILE MEMORY UNIT
91
2
120
1
4
80A
80B
91A
91B
60a
CHANNEL UNIT
CONTROL PROCESSOR
3
60b
70a
70b
60c
70c
60d
5
CONTROL UNIT
60
CPU
61
70d
70
61a
DKU
CHANNEL UNIT
71
71a
61b
71b
61c
71c
61d
CONTROL UNIT
CONTROL PROCESSOR
71d
81A
81B
90A
90B
5
CACHE UNIT
NONVOLATILE MEMORY UNIT
111
81
90
121
CONTROL PROCESSOR

FIG. 6

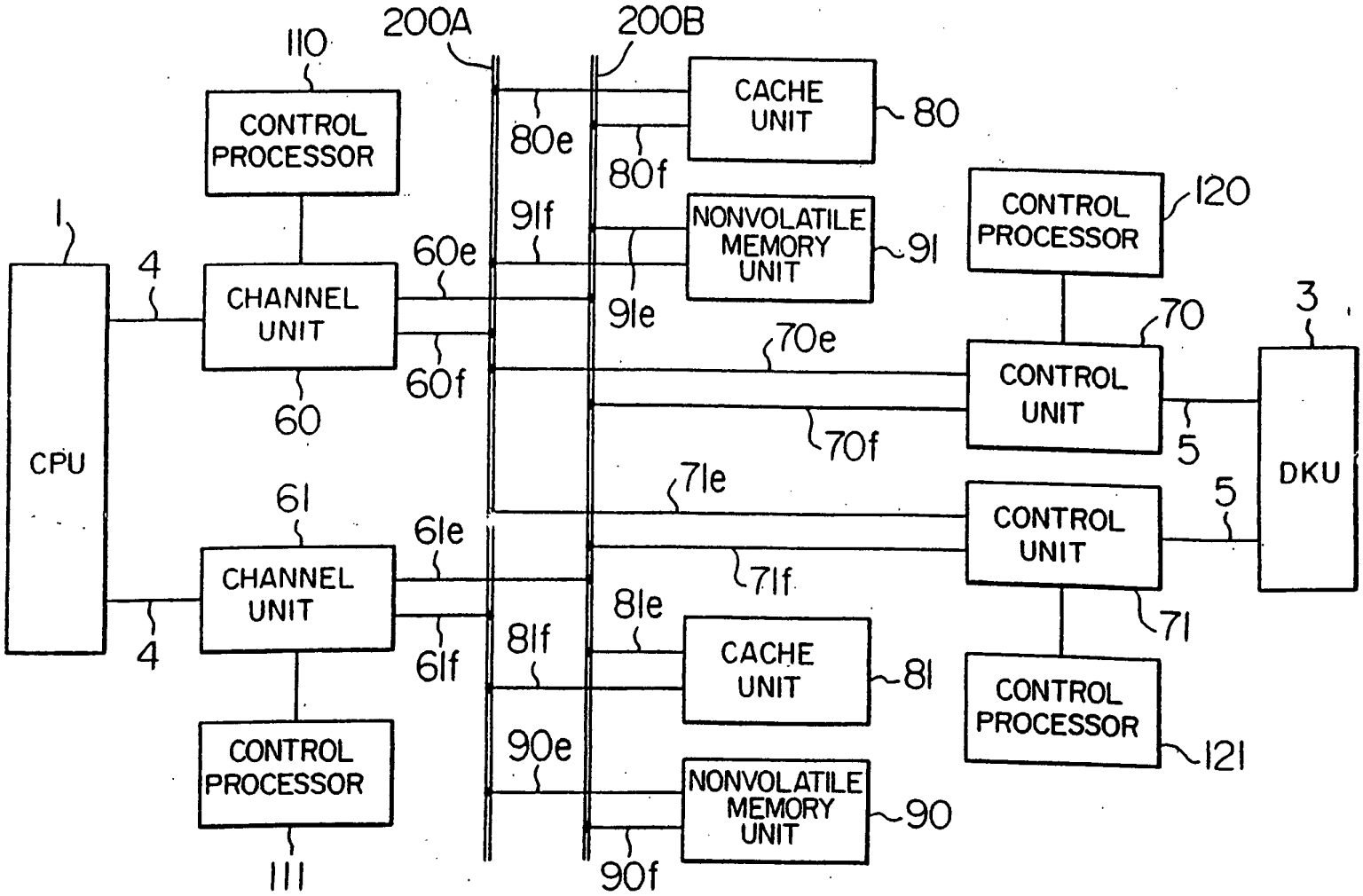
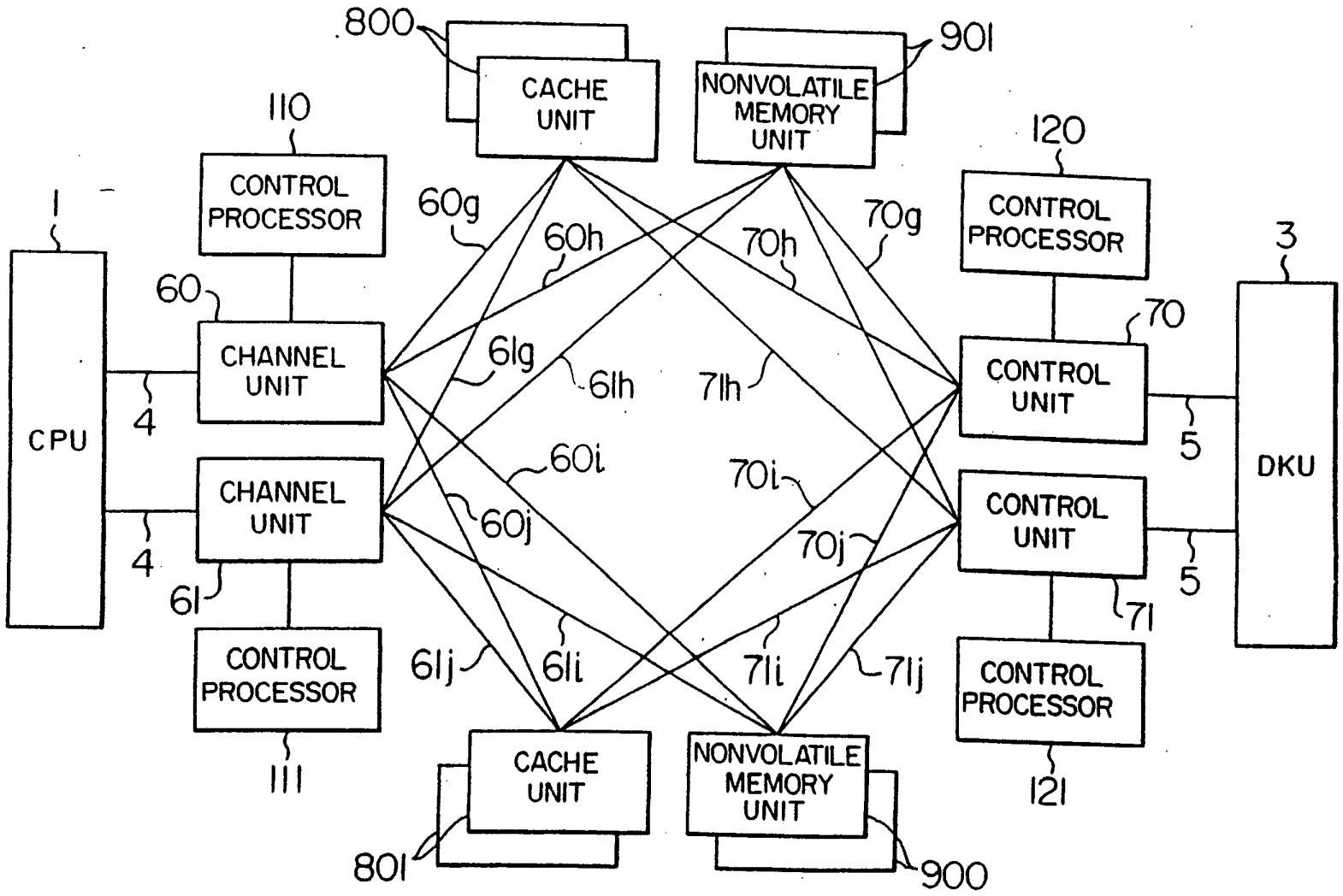

200A
200B
110
CONTROL PROCESSOR
80e
80f
CACHE UNIT
80
1
CPU
4
CHANNEL UNIT
60e
60f
60
91f
91e
NONVOLATILE MEMORY UNIT
91
120
CONTROL PROCESSOR
70
3
70e
70f
CONTROL UNIT
5
DKU
61
CHANNEL UNIT
61e
61f
71e
71f
CONTROL UNIT
71
81e
81f
CACHE UNIT
81
90e
90f
NONVOLATILE MEMORY UNIT
90
CONTROL PROCESSOR
111
121

FIG. 7


800
CACHE UNIT
901
NONVOLATILE MEMORY UNIT
110
CONTROL PROCESSOR
120
CONTROL PROCESSOR
1
CPU
60g
60h
70h
70g
3
DKU
60
CHANNEL UNIT
61g
61h
71h
70
CONTROL UNIT
4
5
60i
70i
CHANNEL UNIT
60j
70j
CONTROL UNIT
4
5
61
71
CONTROL PROCESSOR
61j
61i
71i
71j
CONTROL PROCESSOR
111
121
CACHE UNIT
NONVOLATILE MEMORY UNIT
801
900